**CLASS – 12**

**WORKSHEET- SEMICONDUCTOR DEVICES AND DIGITAL CIRCUITS**

## A. SEMICONDUCTOR MATERIAL

**(1 Mark Questions)**

1. Give the ratio of holes and the number of conduction electrons in an intrinsic semiconductor.

Sol. The ratio of the number of holes to the number of conduction electrons in an intrinsic semiconductor is 1.

2. How does the forbidden energy gap of an intrinsic semiconductor vary with increase in temperature?

Sol. As we increase the temp, electrons from the top of the valence band would gain thermal energy and gets excited into the C.B, so band gap would decrease with increase in temp. Hence forbidden energy gap of a semiconductor decreases with increase in temperature.

3. How does the energy gap in an intrinsic semiconductor vary, when doped with a pentavalent impurity?

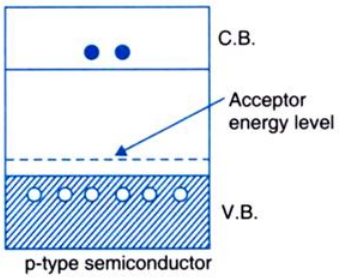
Sol. When an intrinsic semiconductor is doped with the impurity atoms of valence five like As, P or Sb, some addition energy levels are produced, situation in the energy gap slightly below the conduction band which are called donor energy levels. Due to it, energy gap in semiconductor decreases

4. Is the ratio of number of holes and number of conduction electrons in a p-type semiconductor more than, less than or equal to 1?

Sol. The ratio of number of holes and number of conduction electrons in a p-type semiconductor is less than 1.

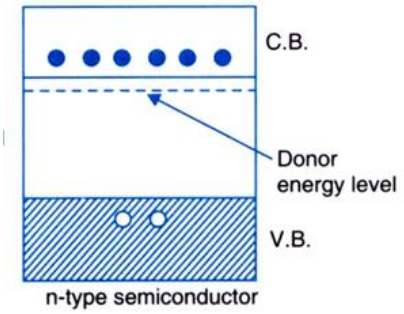
5. Draw the energy band diagram of p-type semiconductor

Sol.




6. Draw the energy band diagram of n-type semiconductor

Sol.




7. What are 'holes'?

Sol. In physics, a hole is an electric charge carrier with a positive charge, equal in magnitude but opposite in polarity to the charge on the electron.

8. Carbon, silicon and germanium have four valence electrons each. These are characterised by valence and conduction bands separated by energy band gap respectively equal to (Eg)c, (Eg)si and (Eg)Ge-
Which of the following statements is true ?
(a) (Eg)Si < (Eg)Ge < (Eg)c
(b)(E)c<(Eg)Ge>(Eg)si
(c) (Eg)c > (Eg)si > (Eg)Ge
(d) (Eg)c = (Eg)si = (Eg)Ge

Ans. (c)
Out of the given three elements, energy band gap is maximum for carbon, less for silicon and least for germanium.

9. The conductivity of a semiconductor increases with increase in temperature because
(a) number density of free current carriers increases.
(b) relaxation time increases.
(c) both number density of carriers and relaxation time increase.
(d) number density of current carriers increases, relaxation time decreases but effect of decrease in relaxation time is much less than increase in number density

Ans. (d)
In semiconductor the density of charge carriers (electron hole) are very small, so its resistance is high when the conductivity of a semiconductor increases with increase in temperature, because the number density of current carries increases then the sped of free electron increase and relaxation time decreases but effect of decrease in relaxation is much less than increase in number density.

**(2 Marks Questions)**

10. What is meant by the terms, doping of an intrinsic semiconductor? How does it affect the conductivity of a semiconductor?

Sol. Doping is the process of adding impurities to intrinsic semiconductors to alter their properties. Normally Trivalent and Pentavalent elements are used to dope Silicon and

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Germanium. When an intrinsic semiconductor is doped with Trivalent impurity it becomes a p−Type semiconductor.

11. Explain with the help of graph, the variation of conductivity with temperature for a metallic conductor

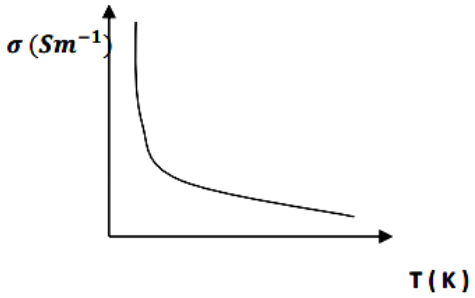
Sol. Conductivity of a metallic conductor is : $\sigma = 1/\rho = ne^2\tau/m$

For a metal, The number density of electrons 'n' is fixed.

When temperature of metal increases, the amplitude of vibrations of the atoms or ions of the metal conductor increases.

As a result of it, the collision of electrons with atoms/ ions become more frequent, consequently, the relaxation time 'τ' decreases. It means, Conductivity of a metallic conductor decreases.

It means, conductivity of a metallic conductor decreases with the increase of temperature.




12. Distinguish between metals, insulators and semiconductors on the basis of their energy bands.

Sol. The points of differences between metals, insulators, and semiconductors are as follows:

| Metal | Insulator | Semiconductor |
|---|---|---|
| • Metals are the substances that are naturally found below the earth. | • Insulators are poor conductor of heat and electricity. | • A substance that holds the property of both conductor and insulators are known as semiconductors. |
| • The conduction band in metals is either filled or partially filled while the valence band is partially empty.<br>• The electrons move from low energy to high energy where they behave as free | • The valence band is completely filled while the conduction band is partially filled. | • The valence band is completely filled while the conduction band is empty in the case of semiconductors. |

electrons.

- There is no forbidden gap in the case of metals.
- As a result there is large energy gap.
- This results in low gap in energy bands.

13. A semiconductor has equal electron and hole concentration $6\times10^{8}$ $m^{-3}$. On doping with certain impurity, electron concentration increases to $8\times10^{12}$ $m^{-3}$. Identify the type of semiconductor doping

Sol. $n_i = 6 \times 10^8/ m^3$ and $n_e = 8 \times 10^{12}/m^3$
$n_e > n_1$ so it is N-type semiconductor.

14. A semiconductor has equal electron and hole concentration of $6\times10^{8}/m^3$. On doping with certain impurity, electron concentration increases to $9\times10^{12}/m^3$.
(i) Identify the new semiconductor obtained after doping.
(ii) Calculate the new hole concentration.

Sol. (i) $n_i = 6 \times 10^8/ m^3$ and $n_e = 9 \times 10^{12}/m^3$
$n_e > n_1$ so it is N-type semiconductor.
(ii) $\because n_i^2 = n_e n_h$, $n_h = n_i^2/n_e = 36 \times 10^{16}/9 \times 10^{12} = 4 \times 10^4/m^3$

15. Distinguish between an intrinsic semiconductor and P-type semiconductor.
Given reason, why, a P-type semiconductor crystal is electrically neutral, although $n_h >> n_e$?

Sol.

| | Intrinsic Semiconductor | Extrinsic semiconductor |
|---|---|---|
| (i) | It is a semiconductor in pure form | It is a semiconductor doped with a trivalent (like Al, In) impurity. |
| (ii) | Intrinsic charge carriers are electrons and holes with equal concentration. | Majority charge carriers are holes and minority charge carriers are electrons. |
| (iii) | Conductivity depends on temperature | Conductivity depends on temperature as well as dopant concentration. |

In p type semiconductor, trivalent impurity is doped with tetravalent pure semiconductor. Both type of atom (impurity and host semiconductor) are electrically neutral and hence, so produced p type semiconductor is electrically neutral.

16. How is a p-type semiconductor formed? Name the major charge carriers in it. Draw the energy band diagram of a p-type semiconductor.

Sol. The extrinsic p-Type Semiconductor is formed when a trivalent impurity is added to a pure semiconductor in a small amount, and as a result, a large number of holes are created in it. A large number of holes are provided in the semiconductor material by the addition of trivalent impurities like Gallium and Indium.

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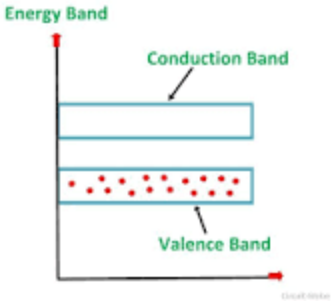
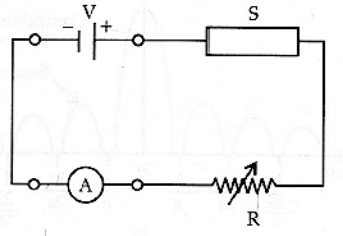



**(3 Marks Questions)**

17. The diagram shows a piece of pure semiconductor, S in series with a variable resistor R, and a source of constant voltage V. Would you increase or decrease the value of R to keep the reading of ammeter (A) constant, when semiconductor S is heated? Give reason.




Sol. Value of R should be increased with the increase in temperature of semiconductor as circuit resistance decreases and current tends to increase.

18. A semiconductor has equal electron and hole concentrations of $2\times10^{8}/m^{3}$. On doping with a certain impurity, the hole concentration increases to $4\times10^{10}/m^{3}$.
(i) What type of semiconductor is obtained on doping?
(ii) Calculate the new electron concentration of the semiconductor.
(iii) How does the energy gap vary with doping?

Sol.

(i) Since hole concentration increases on doping, semi-conductor is a p-type

(ii) $n_i^2 = n_e \times n_h$

Where $n_i$ is the intrinsic concentration

$$\left(2\times10^{8}\right)^2 = n_e \times 4\times10^{10}$$

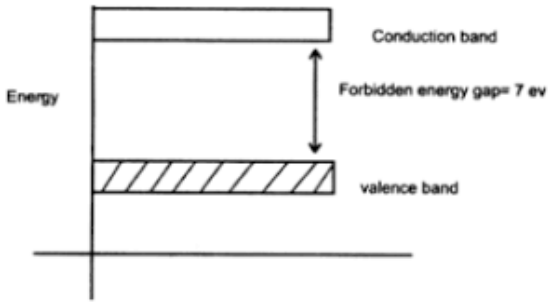
$$n_e = 10^{6}\ m^{-3}$$

(iii) Energy gap decreases with doping as acceptor levels get created between valence band and conduction band.

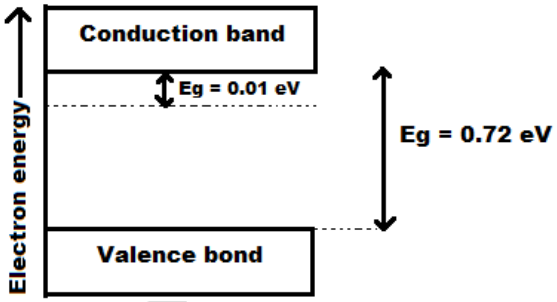
19. Explain the formation of energy band in solids. Draw energy band diagram for (i) a conductor, (ii) an intrinsic semiconductor.

Sol. In solids, molecules are arranged in a way in which atoms tend to move into the orbits of the atoms which are close to them. Therefore, orbits of electrons overlap when atoms come together. **By intermixing atoms in the solid state, several bands of energy levels are formed**. These energy levels are called Energy Bands.

(i)



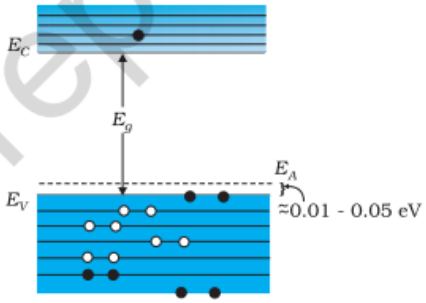

(ii)




20. What is an intrinsic semiconductor? How can this material be converted into (i) p-type (ii) n-type extrinsic semiconductor? Explain with the help of energy band diagrams.

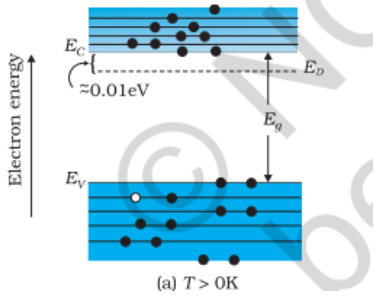
Sol. Semiconductors in which the number of electrons $n_e$ is equal to the number of holes $n_h$ are intrinsic semiconductors. When a small amount of suitable impurity is added to the intrinsic semiconductor we can convert it into an extrinsic semiconductor of either p-type or n-type.

Energy band diagram of p-type semiconductor.




(b) $T > 0K$

Energy band diagram of n-type semiconductor




21. Deduce an expression for the conductivity of p-type semiconductor.

_____
_____
_____
_____
_____
_____

**(5 Marks Questions)**

22. On the basis of the energy band diagrams, distinguish between (a) a metal, (b) an insulator and (iii) a semiconductor

Sol. Same as 12.

## B. SEMICONDUCTOR DEVICE

**(1 Mark Questions)**

1. How does the width of the depletion region of pn junction vary, if the reverse bias applied to it increases?

Sol. Under reverse biasing the applied potential difference causes a field which is in the same direction as the field due to internal potential barrier. This results in an increase in barrier voltage and hence the width of depletion layer decreases.

2. In the following diagrams, write which of the diodes are forward biased and which are reverse biased.

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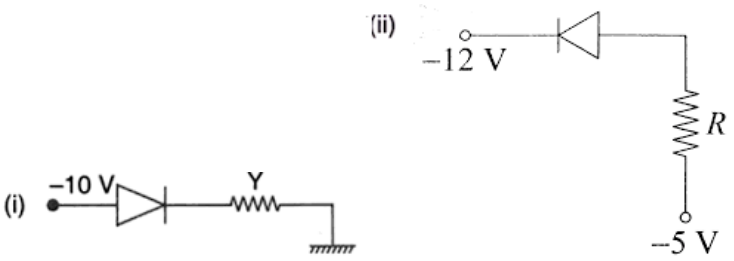
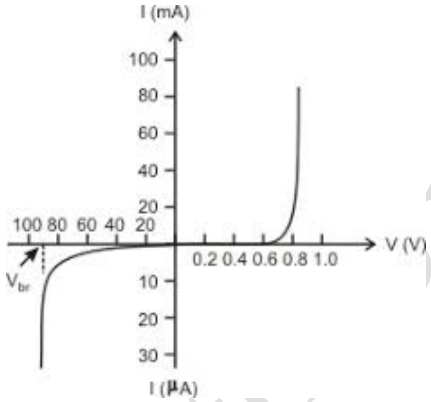



Sol. (i) is reverse biased and (ii) is forward biased.

3. The figure below shows the V-I characteristic of a semiconductor diode.

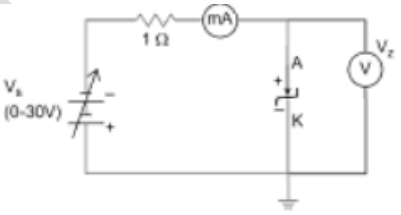



(i) Identify the semiconductor diode used

Sol. The semiconductor diode whose V-I characteristic is shown in the figure is Zener diode.

(ii) Draw the circuit diagram to obtain the given characteristic of this device

Sol.




(iii) Briefly explain how this diode can be used as a voltage regulator

Sol. When forward biased, it behaves like a normal signal diode, but when the reverse voltage is applied to it, the voltage remains constant for a wide range of currents. Due to this feature, it is used as a voltage regulator in d.c. circuit.

4. Draw the voltage current characteristic of a Zener diode.

Sol.

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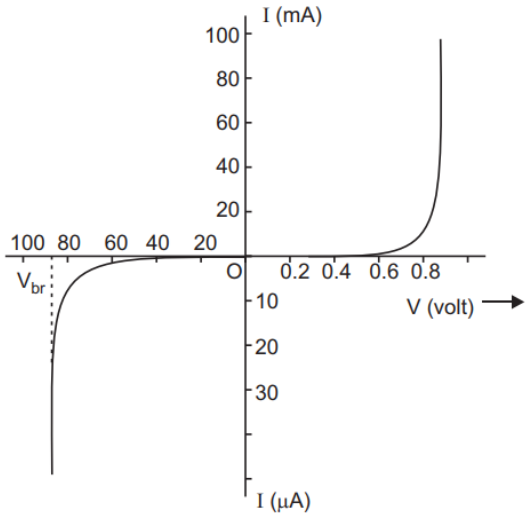



5. Why should a photodiode be operated at reverse bias?

Sol. A photodiode is used to detect optical signals. The fractional change in the minority carrier dominated reverse bias current due to the photoeffect is more easily measurable than fractional change in forward bias current. Hence a photodiode is preferably operated in reverse bias condition.

6. State the reason, why GaAs is most commonly used in making of a solar cell.

Sol. GaAs (gallium arsenide) is most commonly used in making of a solar cell, because it absorbs relatively more energy from the incident solar radiations having relatively higher absorption co-efficient.

7. In an n-type silicon, which of the following statement is true :
(a) Electrons are majority carriers and trivalent atoms are the dopants.
(b) Electrons are minority carriers and pentavalent atoms are the dopants.
(c) Holes are minority carriers and pentavalent atoms are the doplants.
(d) Holes are majority carriers and trivalent atoms are the dopants.

Ans. (c)

8. Which of the statements given in previous Question is true for p-type semiconductors?

Ans. (d)

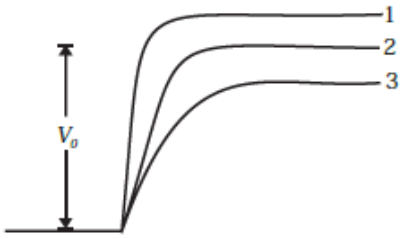
9. In an unbiased p-n junction, holes diffuse from the p-region to n-region because
(a) free electrons in the n-region attract them.
(b) they move across the junction by the potential difference.
(c) hole concentration in p-region is more as compared to n-region.
(d) All the above.

Ans. (c)

10. When a forward bias is applied to a p-n junction, it
(a) raises the potential barrier
(b) reduces the majority carrier current to zero
(c) lowers the potential barrier
(d) none of the above.

Ans. (c)

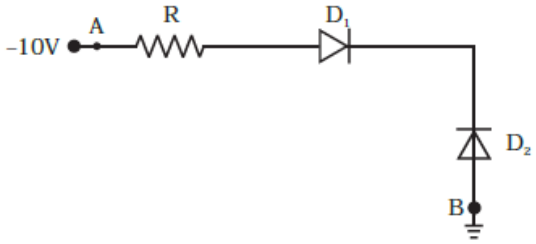
11. In Figure, $V_0$ is the potential barrier across a p-n junction, when no battery is connected across the junction




(a) 1 and 3 both correspond to forward bias of junction
(b) 3 corresponds to forward bias of junction and 1 corresponds to reverse bias of junction
(c) 1 corresponds to forward bias and 3 corresponds to reverse bias of junction.
(d) 3 and 1 both correspond to reverse bias of junction

Ans. (b)
When p-n junction is forward biased then the depletion layer is compresses or decrease so it opposes the potential junction resulting decrease in potential barrier junction when p-n junction is reverse biased, it supports and potential barrier junction, resulting increase in potential across the junction.

12. In Figure, assuming the diodes to be ideal,




(a) $D_1$ is forward biased and $D_2$ is reverse biased and hence current flows from A to B
(b) $D_2$ is forward biased and $D_1$ is reverse biased and hence no current flows from B to A and vice versa.
(c) $D_1$ and $D_2$ are both forward biased and hence current flows from A to B.
(d) $D_1$ and $D_2$ are both reverse biased and hence no current flows from A to B and vice versa.

Ans. (b)
As the given circuit, p-side of p-n junction $D_1$ is connected to lower voltage and n side of $D_1$ of higher voltage.
So $D_1$ is reverse biased.

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In the circuit A is at -10V and B is at 0(zero) V. So B is positive then A or The p side of p-n junction $D_2$ is at higher potential and n-side of $D_2$ is at lower potential. So $D_2$ is forward biased.
Hence, no current flows through the junction B to A and vice versa.

13. The output of the given circuit in Figure.

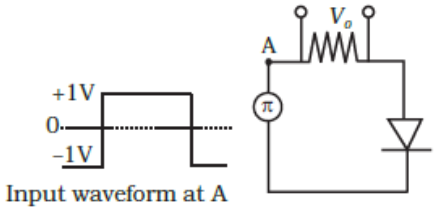

(a) would be zero at all times.
(b) would be like a half wave rectifier with positive cycles in output.
(c) would be like a half wave rectifier with negative cycles in output.
(d) would be like that of a full wave rectifier

Ans. (c)
When the diode will be forward biased during positive half cycle of input AC voltage, the resistance of p-n junction is low. The current in the circuit is maximum. So, a maximum potential difference will appear across resistance connected in a series of circuit. So, potential across PN junction will be zero. When the diode will be in reverse biased during negative half cycle of AC voltage, the resistance of p-n junction becomes high which will be more than resistance in series. So, there will be voltage across p-n junction with negative cycle in output.

14. Can the potential barrier across a p-n junction be measured by simply connecting a voltmeter across the junction?

Sol. We cannot measure the potential barrier across p-n junction by voltmeter because the voltmeter must have a resistance very high compared to the junction resistance, the latter being nearly infinite.

15. Draw the output waveform across the resistor (Figure).




Sol. In given circuit waveform is connected at A and waveform obtained across resistance diode conducts when diode is in forward biased so output will be only when input is +1V is between $t_1$ and $t_2$. So output waveform will be only $t_1$ to $t_2$ which is in given figure.



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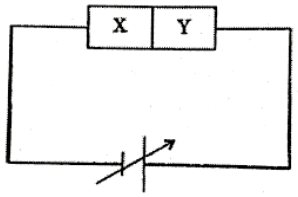
**(2 Marks Questions)**

16. Explain how the width of depletion layer in a pn junction diode changes when the junction is (i) forward biased (ii) reverse biased.

Sol. (i) The width of depletion layer of a p-n junction decreases when the junction is forward biased. (ii) The width of depletion layer of a p-n junction increases when the junction is reverse biased.

17. Two semiconductor materials X and Y shown in the given figure, are made by doping germanium crystal with indium and arsenic respectively. The two are joined end to end and connected to a battery as shown.

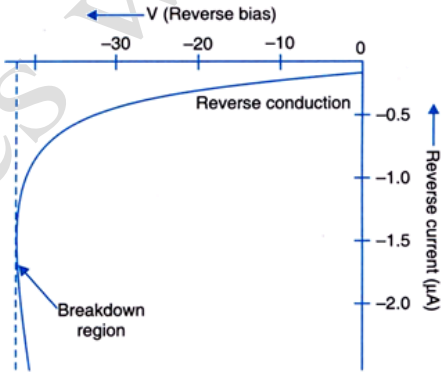



(i) Will the junction be forward biased or reverse biased?

(ii) Sketch a V-I graph for this arrangement.

Sol. (i) X is a p type semiconductor and Y is n type semiconductor. So the junction is reverse biased.

(ii)




18. Draw the circuit diagram of p n junction diode in forward bias. Sketch the voltage current graph

Sol.

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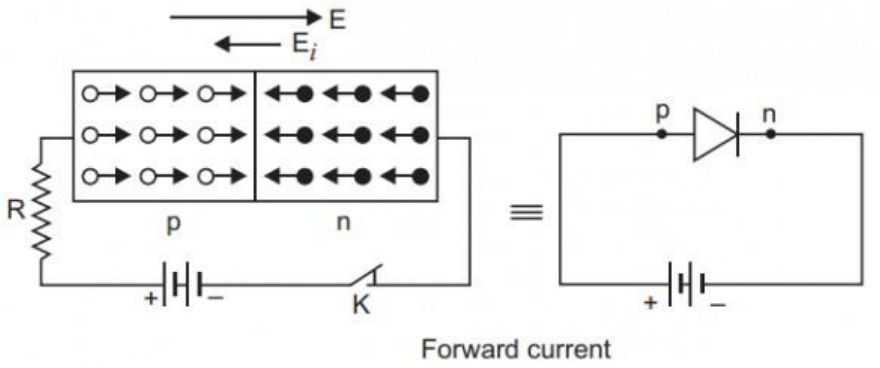
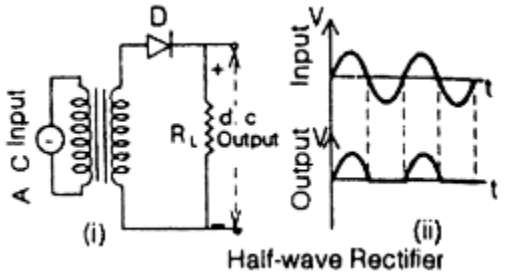



19. Explain the use of pn diode as rectifier

Sol. The main application of p-n junction diode is in rectification circuits. These circuits are used to describe the conversion of a.c signals to d.c in power supplies. Diode rectifier gives an alternating voltage which pulsates in accordance with time.

20. Draw the circuit diagram for use of pn junction as a half wave rectifier

Sol.

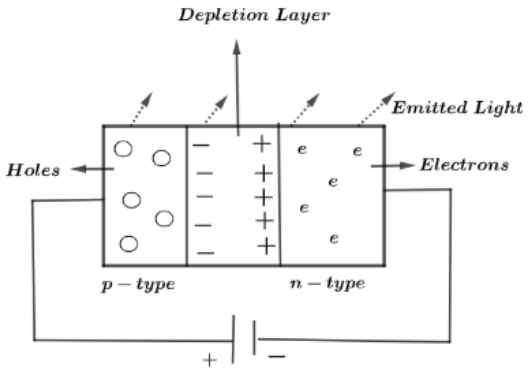



21. What is a pn junction diode? Define the term dynamic resistance for the junction diode.

Sol. A p-n junction diode allows electric current in one direction and blocks electric current in another direction. It allows electric current when it is forward biased and blocks electric current when it is reverse biased. However, no diode allows electric current completely even in forward biased condition.

22. With the help of a diagram, show the biasing of a light emitting diode (LED). Give its two advantages over conventional incandescent lamps.

Sol. A diagram which shows the biasing of Light Emitting Diode (LED).

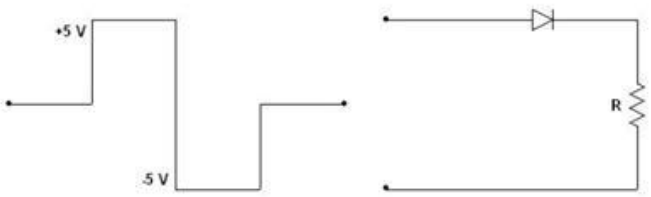



Advantages of Light emitting diode over incandescent lamp:

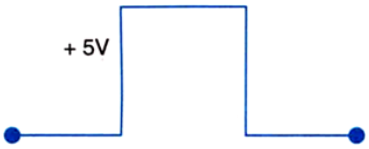
1.Since Light Emitting Diode works on the principle of Semiconductors hence LEDs are much more energy efficient than incandescent lamps and hence are generally used in households for low power generating.

2.Very effective maintenance. Since LEDs are replaceable which minimizes its cost and hence it's eco-friendly and no harm to the environment as compared to ordinary lamps.

23. Draw and explain the output waveform across the load resistor R, if the input waveform is as shown in the given figure.




Sol. When the input is +5V, the diode gets forward biased, the output across R is +5V, as shown in figure. When the input voltage is – 5V, the diode gets reverse biased. No output is obtained across R.




24. In half-wave rectification, what is the output frequency if the input frequency is 50 Hz. What is the output frequency of a full-wave rectifier for the same input frequency.

Sol. Input frequency = 50 HzFor a half-wave rectifier, the output frequency is equal to the input frequency.

∴ Output frequency = 50 Hz

For a full-wave rectifier, the output frequency is twice the input frequency.

∴ Output frequency =2×50=100 Hz

25. A p-n photodiode is fabricated from a semiconductor with band gap of 2.8 eV. Can it detect a wavelength of 6000 nm?

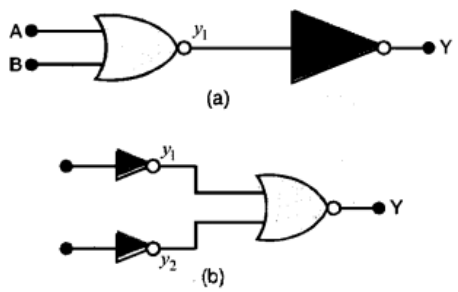
Sol. Energy required to cross the band gap, $E_g$ = 2.8eV

Wavelength of incident photon, $\lambda = 6000nm = 6\times10^{-6}m$

Energy of incident photon = $\frac{hc}{\lambda} = \frac{6.63\times10^{-34}\times3\times10^{8}}{6\times10^{-6}}$ = 0.207eV

At $E < E_g$, the p-n junction cannot detect the radiation of wavelength 6000nm.

26. You are given the two circuits as shown in Figure. Show that circuit (a) acts as OR gate while the circuit (b) acts as AND gate.




Sol. (a) In figure a, the first gate in a NOR gate which gives high output when both its inputs are low. Its output is then fed to a NOT gate. So we can write the truth table as:

| **A** | **B** | **A+B** | **$Y=\overline{A+B}$** | **$Y = \bar{Y}$'** |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |

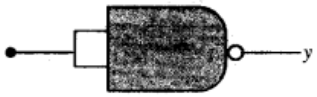
Clearly Y = A +B. Hence the circuit acts as an OR gate.

(b) In figure b, the inputs of two NOT gages are fed to a NOR gate. The NOR gate gives high output and when both its inputs are low. So we can write the truth table as:

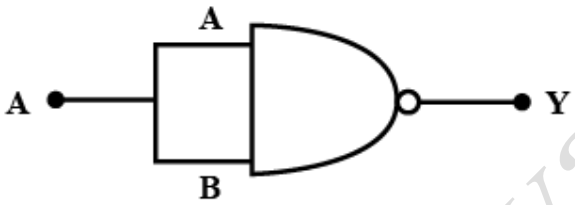
| **A** | **B** | **$\bar{A}$** | **$\bar{B}$** | **$\bar{A}+\bar{B}$** | **$Y=\overline{A+B}$** |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

Clearly Y = A+B,. Hence the circuit acts as AND gate.

27. Write the truth table for a NAND gate connected as given in Fig. Hence identify the exact logic operation carried out by these circuits.




Sol.

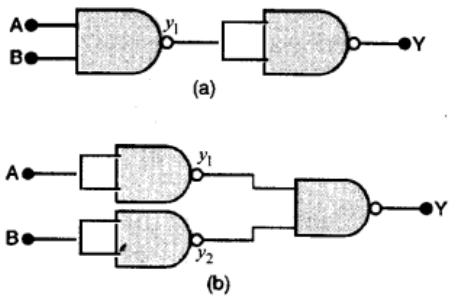



**The truth table of NAND gate is as given below:**

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 1 | 0 |

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

28. You are given two circuits as shown in Fig., which consist of NAND gates. Identify the logic operation carried out by the two circuits.




Sol. (a) In figure a, the first gate is a NAND gate. Its output is fed to a NOT gate (made from a NAND gate). The output is low when both the inputs are high. So we can write the truth table as:

| A | B | A.B | $Y=\overline{A.B}$ | $Y = \overline{Y}$' |
|---|---|---|---|---|

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| | | | | |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |

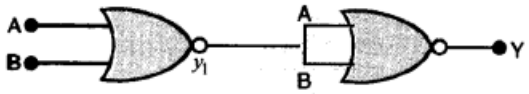
Clearly, input Y = A +B. Hence the given circuit performs the function of AND gate.

(b) In figure b, the inputs of two NOT gates (made from NAND gates) are fed to a NAND gate. The output of a NAND gate is low when both the inputs are high. So we can write the truth table as

| **A** | **B** | $\overline{A}$ | $\overline{B}$ | $\overline{A}.\overline{B}$ | $Y=\overline{A.B}$ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |

Clearly output Y = A+B. Hence the given circuit performs the function of an OR gate.

29. Write the truth table for circuit given in the Fig. below consisting of NOR gates and identify the logic operation (OR, AND, NOT) which this circuit is performing.

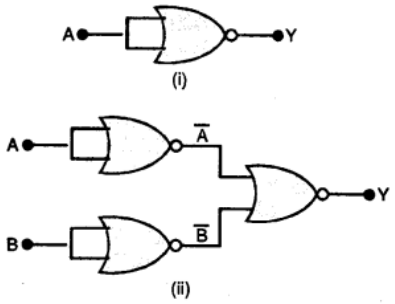



Sol. The first gate is a NOR gate. The second gate is also a NOR gate with both the input terminals connected together. The logic table for the above circuit is as follows:

| **First NOR gate** | | | | **Second NOR gate** | | |
|---|---|---|---|---|---|---|
| **A** | **B** | **A+B** | $Y'=\overline{A+B}$ | **A=Y'** | **B=Y'** | $Y=\overline{A+B}$ |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

Clearly $Y = \overline{A+B} = A + B$. Thus the given circuit performs OR function.

30. Write the truth table for the circuits given in the Fig., consisting of NOR gates only. Identify the logic operations (OR, AND, NOT) performed by the two circuits.




Sol. (a) The circuit of fig a is a NOR gate with both the input terminals connected together. The output of a NOR gate is high when both its inputs are low. Keeping this in mind, we can write the truth table as:

| **A** | **B** | **$Y=\overline{A+B}$** |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 1 | 0 |

Clearly $Y=\overline{A+B}=\overline{A}$

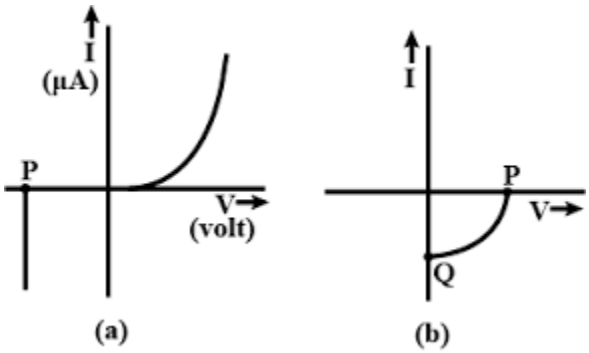
Hence a NOR gate with both its input terminals connected together performs the BOT operation.

(b) Here the inputs A and B get inverted by the two NOT gats (made from NOR gates). The inputs $\overline{A}$ and $\overline{B}$ are fed to a NOR gate. The output of a NOR gate is high when both the inputs are low. So we write the truth table as:

| **A** | **B** | **$\overline{A}$** | **$\overline{B}$** | **$\overline{A}+\overline{B}$** | **$Y=\overline{A+B}$** |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

Clearly $Y=\overline{A+B}$ = A.B. Hence the circuit of figure b performs the function of an AND gate.

31. (i) Name the type of a diode whose characteristics are shown in Fig. (a) and Fig. (b). (ii) What does the point P in Fig. (a) represent? (iii) What does the points P and Q in Fig. (b) represent?

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Sol. (i) Figure a) depicts the Zener diode's characteristics, whereas figure b) depicts the solar cell. ii) In Figure a), point P denotes the Zener breakdown voltage. iii) Point Q in Figure b) represents zero voltage and negative current.

32. Explain why elemental semiconductor cannot be used to make visible LEDs.

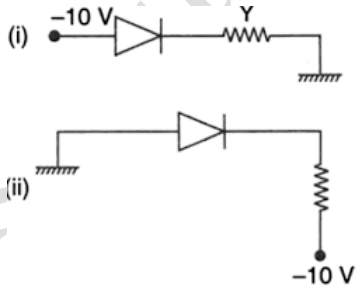
Sol. In elemental conductor, the band gap is such that the emissions are in infrared region and not in visible region. Because the energy released by combination of holes and electrons in elemental semiconductors does not lie in the visible spectrum, elemental semiconductor cannot be used to make visible LED's .

**(3 Marks Questions)**

33. Explain how the depletion layer and barrier potential are formed in a pn junction diode.

Sol. the formation of pn junction, the holes from p-region diffuse into the M-region and electrons from n-region diffuse into p-region and electron hole pair combine and get annihilated. This in turn, produces potential barrier VB across the junction which opposes the further diffusion through the junction.

34. Explain with the help of a circuit diagram, how the thickness of depletion layer in a p-n junction diode changes when it is forward biased. In the following circuits which one of the two diodes is forward biased and which is reverse biased?

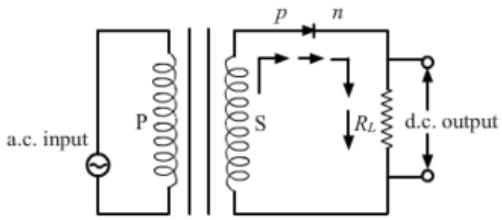



Sol. When applied voltage is such that n side is negative and p side is positive, the applied voltage is opposite to the barrier potential. Hence the effective barrier potential, becomes $V_B - V$, and the energy barrier across the junction decreases. Thus the junction width decreases.

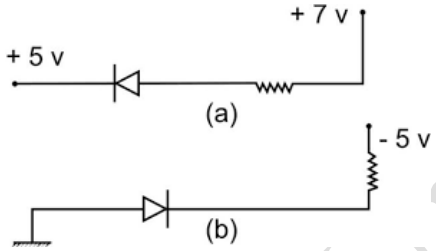
(i) p-n junction is forward biased (ii) p-n junction is reverse biased.

35. Explain (i) forward biasing, (ii) reverse biasing of a p-n junction diode. With the help of a circuit diagram explain the use of this device as a half wave rectifier.

Sol. Forward biasing indicates the application of a voltage across a diode that enables current to flow easily, while reverse biasing means putting a voltage across a diode in the opposite direction.




36. Explain with the help of a circuit diagram, how the thickness of depletion layer in a p-n junction diode changes when it is forward biased. In the following circuits which one of the two diodes is forward biased and which is reverse biased?




37. Explain briefly with the help of circuit diagram, how V-I characteristics of a pn junction diode are obtained in (i) forward bias and (ii) reverse bias. Draw the shape of curves obtained.

Sol. Referring to the characteristic curve,

The VI characteristic curve of p-n junction diode in forward biased is non linear.

The current first increases slowly,almost negligibly,till the voltage across the diode crosses a certain value.

After the characteristic voltage,the diode current increases significantly,even for a very small increase in the diode bias voltage.This voltage is called THRESHOLD VOLTAGE or CUT-IN voltage.

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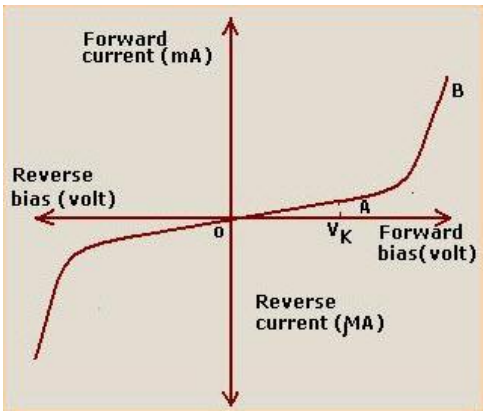
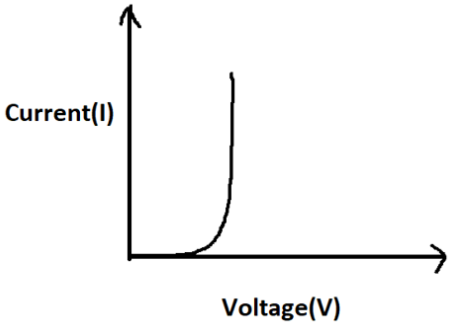
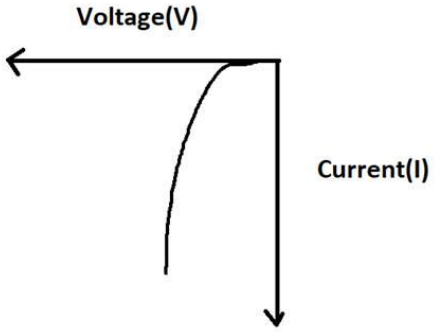



Curves obtained in forward biased:




Curve obtained in reverse biased:




38. Explain with the help of a schematic diagram, the principle and wording of a Light Emitting Diode. What criteria is kept in mind while choosing the semiconductor material for such a device? Write any two advantages of Light Emitting Diode over conventional incandescent lamps

Sol. Light emitting diode is a type of semiconductor device in which when current flows through it. Diode emits photons which in result produce light. When current and the material of a semiconductor combine it produces light in the device.

Let us first draw a diagram which shows the biasing of Light Emitting Diode (LED).

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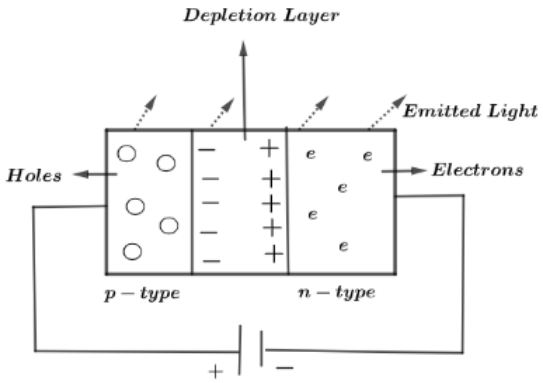



In p-type region Holes are present and in n-type region there are electrons and when battery is connected in forward biasing such that positive terminal of battery connected to p-type region and negative terminal of battery connected with n-type region, this is called forward biasing. The thickness of the depletion layer becomes narrow and light is emitted through the semiconductor device.

Advantages of Light emitting diode over incandescent lamp:

1.Since Light Emitting Diode works on the principle of Semiconductors hence LEDs are much more energy efficient than incandescent lamps and hence are generally used in households for low power generating.

2.Very effective maintenance. Since LEDs are replaceable which minimizes its cost and hence it's eco-friendly and no harm to the environment as compared to ordinary lamps.

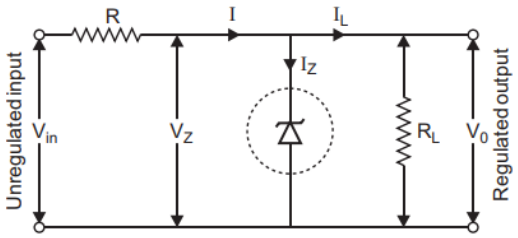
39. What is Zener diode? How is it symbolically represented? With the help of a circuit diagram, explain the use of Zener diode as a voltage stabilizer.

Sol. A Zener diode is a heavily doped semiconductor device that is designed to operate in the reverse direction.A Zener diode not only allows current to flow from anode to cathode but also, in the reverse direction on reaching the Zener voltage. Due to this functionality, Zener diodes are the most commonly used semiconductor diodes. In this article, let us learn the function of Zener diodes along with its construction, operation and more.

Its symbolic representation is

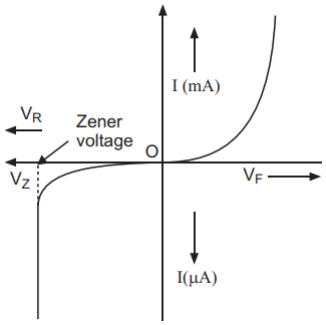
The Zener diode makes its use as a voltage regulator due to the following property :

When a Zener diode is operated in the breakdown region, the voltage across it remains practically constant for a large change in the current. A simple circuit of a voltage regulator using a Zener diode is shown in the figure. The Zener diode is connected across load such that it is reverse biased.




The series resistance R absorbs the output voltage fluctuations so as to maintain constant voltage across the load. If the input dc voltage increases, the current through R and Zener diode also increases. So, voltage drop across R increases, without any change in the voltage across zener diode.

I-V Characteristics




40. Why are photodiodes used preferably in reverse bias condition? A photodiode is fabricated from a semiconductor with band gap of 2.8eV. Can it detect a wavelength of 6000nm? Justify.

Sol. The photodiodes are used in reverse bias condition because the change in reverse current through the photodiode due to change in light flux can be measured easily as the reverse saturation current is directly proportional to the light flux.

Energy band gap of the given photodiode, Eg = 2.8 eV, Wavelength, $\lambda = 6000\ nm = 6000 \times 10^{-9}\ m$

The energy of a signal is given by the relation: $E = hc/\lambda$

Where, h = Planck's constant = $6.626 \times 10^{-34}$ Js,c = Speed of light = $3 \times 10^8$ m/s

$$E = \frac{6.626 \times 10^{-34} \times 3 \times 10^8}{6000 \times 10^{-9}}$$

$= 3.313 \times 10^{-20}$ J

But $1.6 \times 10^{-19}$ J = 1 eV

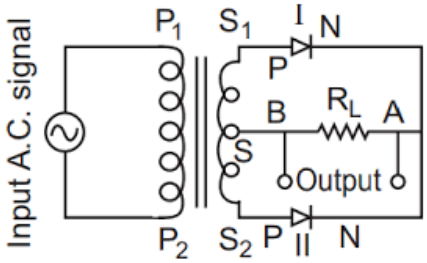
$\therefore E = 3.313 \times 10^{-20}$ J

$$= \frac{3.313 \times 10^{-20}}{1.6 \times 10^{-19}} = 0.207 \text{ eV}$$

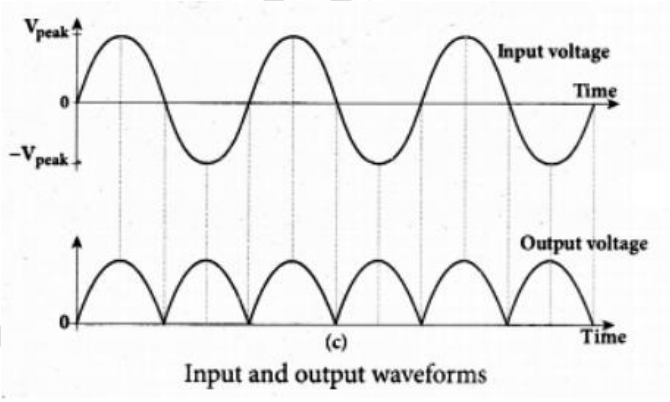
**(5 Marks Questions)**

41. Draw the circuit diagram of a full wave rectifier and explain its working. Draw the input and output waveforms

Sol.




Full wave rectifier is a circuit arrangement which makes use of both half cycles of input alternating current (AC) and convert them to direct current (DC). Thus a full wave rectifier is much more efficient (double+) than a half wave rectifier. This process of converting both half cycles of the input supply (alternating current) to direct current (DC) is termed full wave rectification. Full wave rectifier can be constructed in 2 ways. The first method makes use of a center tapped transformer and 2 diodes.




Input and output waveforms

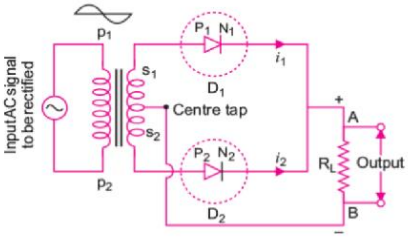
42. State the principle of working of p-n diode as rectifier. Explain, with the help of circuit diagram, the use of p-n diode as fill wave rectifier. Draw a sketch of the input and output waveforms.

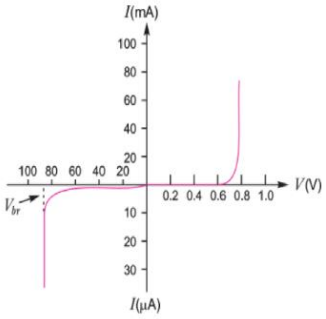
**Sol.** Rectification : Rectifications means conversion of ac into dc. A p-n diodes acts as a rectifier because as ac changes polarity periodically and a p-n diode allows the current to pass only when it is forward biased . This makes the diode suitable for rectification.

Working : The ac input voltage across secondary $S_1$ and $S_2$ changes polarity after each half cycle. Suppose during the first half cycle of input ac signal, the terminal $S_1$ is positive relative to center

tap O and $S_2$ is negative relative O. The diode $D_1$ is forward biased and diode $D_2$ is reversed biased . Therefore, diode $D_1$ conducts while diode $D_2$ does not. The direction of current ($i_1$) due to diode $D_1$ in load resistance RL is directed from A to B in next half cycle, the terminal $S_1$ is negative and $S_2$ is positive relative to center tap O. The diode $_{D1}$ is reverse biased and diode $D_2$ is forward biased. Therefore, diode $D_2$ conducts while $D_1$ does not. The direction of current ($i_2$) due to diode $D_2$ in load resistance RL is still from A to B. Thus , the current in load resistance RL is in the same direction for both half cycles of input ac voltage . Thus for input ac signal the output current is a continuous series of unidirectional pulses.

In a full wave rectifier , if input frequency is f hertz , then output frequency will be 2f hertz because for each cycle of input , two positive half cycles of output are obtained.




## C. LOGIC GATES

### (1 Mark Questions)

1. Write the truth table of OR gate

Sol.

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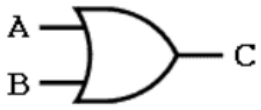
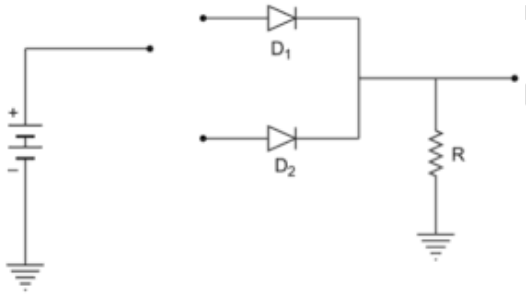
OR




| Inputs | | Output |
|---|---|---|
| A | B | C |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

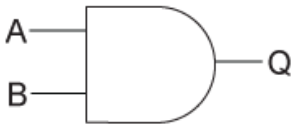
2. Name the logic gate realized using p-n junction diodes in the given diagram. Give its logic symbol.




Sol. OR gate , `y=A+B`. Its logic symbol is shown in Fig.

3. Draw the logic symbol of an AND gate.

Sol.




4. Draw the truth table of an AND gate.

Sol.

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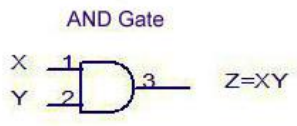
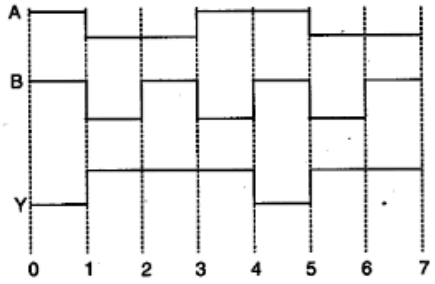



TRUTH TABLE

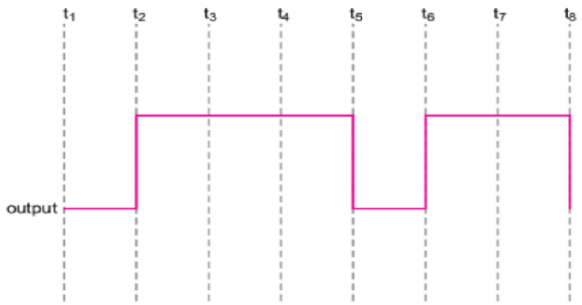
| INPUTS | | OUTPUT |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**(2 Marks Questions)**

5. Draw the output wave form for input wave forms A and B for OR gate.




Sol.




Truth Table

| Input | | Output |
|---|---|---|
| A | B | C |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |


OR Gate

Physics Ujwal ©

6. The following truth table gives the output of a 2-input logic gate:

| A | B | Output |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

If the output of this gate is fed as input to a NOT gate, name the new logic gate so formed.

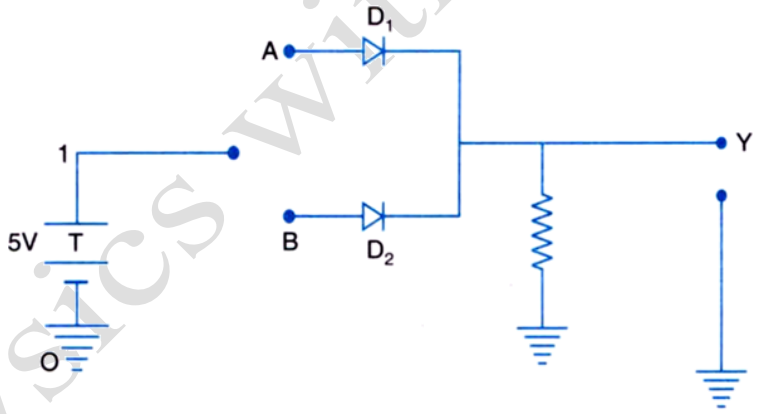
Sol. The new logic gate so formed is OR gate.

7. Draw the input and output wave forms of the signal in a common emitter amplifier using an n-p-n transistor. Write the expression for its voltage gain.

_____
_____
_____
_____

8. Draw a circuit diagram for a two input OR gate and explain its working with the help of input, output waveforms.

Sol.




The negative waveform of a battery is grounded and corresponds to the 0 state and the positive (i.e. 5V voltage in present case) to 1 state.

When both A and B are connected to 0 no current passes through the diode and therefore no voltage develops across R and the output is zero.

When input A is connected to zero and B to 1, the diode $D_2$ is forward biased, and the current through it is limited by a current limiting resistance. The current causes 5 V drop across the resistance assuming the diode to be ideal and this gives an output of 5V or 1. Interchanging A and B to 1 an 0 will still give 5Vdrop across the resistance $D_1$ will conduct. When the terminals A and B are connected to diodes $D_1$ and $D_2$ conduct. However, the voltage drop across R cannot exceed 5V and output is 1.

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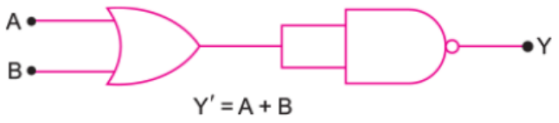
9. The output of an OR gate is connected to both the inputs of a NAND gate. Draw the logic circuit of this combination of gates and write its truth table.

Sol. The truth table is as follows:

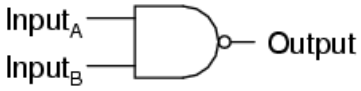
| A | B | Y' | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 |




10. Draw the logic symbol of 2 input NAND gate. Write down its truth table.

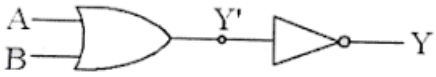
Sol.

*NAND gate*




| A | B | Output |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

11. Name the gate obtained from the combination of gate shown in the figure. Draw its logic symbol. Write the truth table of the combination.




**Sol.** Here the gate P is AND gate and gate Q is NOT gate. The truth table for the combination of the gates is as shown in the figure.

The equivalent gate will be a NAND gate and its truth is shown in the figure.

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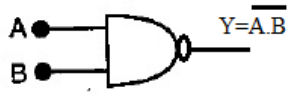
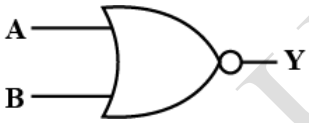
| A | B | X | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |




| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

12. Draw the logic symbol of 2 input NOR gate. Write down its truth table.

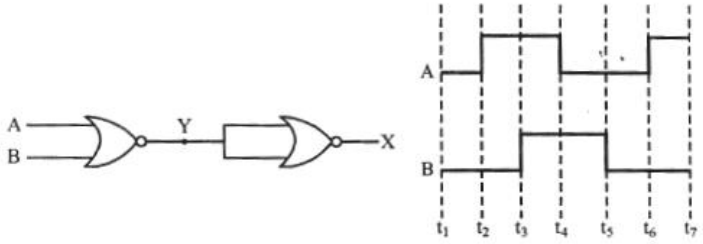
Sol.




Truth table

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

13. Draw the output wave form at X, using the given inputs A and B for the logic circuit shown below. Also identify the gate.




Sol. Same as 2.

14. If the output of a 2 input NOR gate is fed as both inputs A and B to another NOR gate, write down a truth table to find the final output, for all combinations of A, B.

Sol First gate is NOR gate, its output C = bar (A + B).Second gate is also NOR gate, its output

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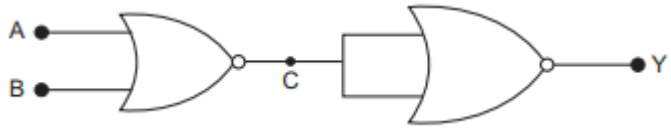
$$Y = \overline{C + C} = \overline{C} \cdot \overline{C} = \overline{C} = \overline{\overline{A + B}} = A + B.$$

This is Boolean expression for OR gate




Its truth table is

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

15. If the output of a 2 input NAND gate is fed as the input to a NOT gate (i) name the new logic gate obtained and (ii) write down its truth table

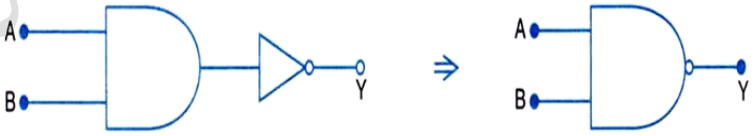
Sol. (i) If the output of two inputs NAND gate is used as the input of NOT gate as shown below, we get back AND gate.

(ii)

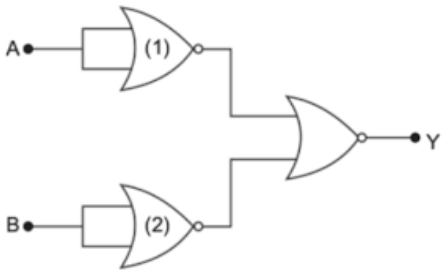
| A | B | Y′ | Y |
|---|---|---|---|
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 |

16. The output of a 2-input AND gate is fed to a NOT gate. Draw the logic circuit of this combination

Sol. The output of a 2 input AND gate is fed to a NOT gate. Give the name of the combination and its logic symbol. Write down its truth table. NAND gate is the combination.




17. The inputs of A and B are inverted by using two NOT gates and their outputs are fed to the NOR gate as shown below:




Analyse the action of the gates (1) and (2) and identify the logic gate of the complete circuit so obtained. Give its symbol and the truth table.

Sol. Output of gate (1), $Y1=A+\bar{A}=A^{-}$

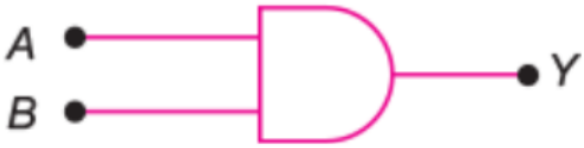
Output of gate (2), $Y2=B+\bar{B}=B^{-}$

Output $Y=Y1+\bar{Y}2=A^{-}+\bar{B}^{-}=A^{--}.B^{--}=AB$

Thus gates (1) and (2) act on 'NOT' gates and the complete circuit acts as 'AND' gate . The symbol and truth table of complete circuit are given below :

Truth table

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |




18. If the output of a 2-input NOR gate is fed as the input to a NOT game, (i) name the new logic gate obtained and (ii) write down its truth table

Sol. (i) Same as 16

(ii) Truth table:

| **A** | **B** | **$Y=\overline{AB}$** |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

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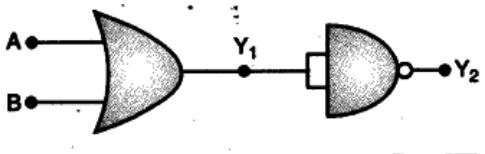
19. Identify the logic gates marked X, y. Write down the output as Z, when A = 1, B = 1 and A = 0, B = 0.


Sol. X is NOR gate and Y is NOT gate: (1,0).

20. For the given circuit given, write truth table showing the outputs $Y_1$:$Y_2$ for all possible inputs at A and B.

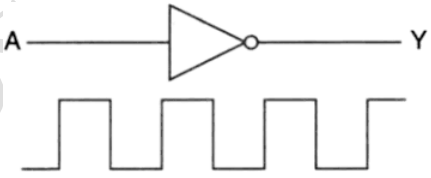



Sol. $Y_1 = A + B$, $Y_2 = \overline{A + B}$

| A | B | $Y_1$ | $Y_2$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

**(3 Marks Questions)**

21. In the figure given below, circuit symbol of a logic gate and input wave form is shown.



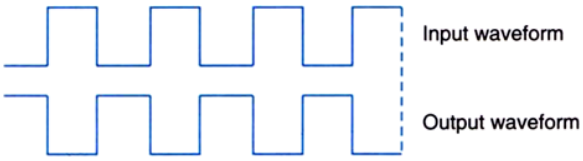

(i) Name the logic gate, (ii) write its truth table and (iii) give the output wave form

Sol. (i) The logic gate is NTO gate.

(ii) Truth Table:

| **Input A** | **Output $\overline{Y} = \overline{A}$** |
|---|---|
| 0 | 1 |
| 1 | 0 |

(iii)

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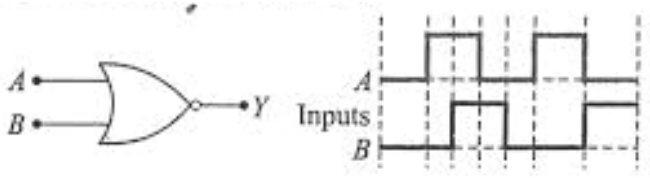
22. In the figure, the circuit symbol of logic gate and input wave forms are given. Name the logic gate. Write its truth table and give the output wave form.




**Sol.** a) OR gate

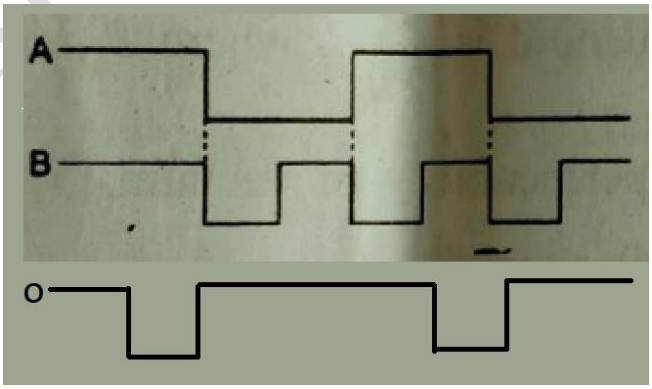
b)The Boolean expression for OR gate is y=A+B. It means, the output of an OR gate will be maximum if one or more inputs will be maximum.

Thus the output waveform will be as showing in Fig. by curve y.

The truth table of OR gates is shown below:

| | A | B | y=A+B |
|---|---|---|---|
| For t1 to t2 | 1 | 1 | 1 |
| For t2 to t3 | 0 | 0 | 0 |
| For t3 to t4 | 0 | 1 | 1 |
| For t4 to t5 | 1 | 0 | 1 |
| For t5 to t6 | 1 | 1 | 1 |
| For t6 to t7 | 0 | 0 | 0 |
| For > t7 | 0 | 1 | 1 |

c) In the figure.

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**D. CASE STUDY**

1. **Band theory of solid:** Consider that the Si or Ge crystal contains N atoms. Electrons of each atom will have discrete energies in different orbits. The electron energy will be same if all the atoms are isolated, i.e., separated from each other by a large distance. However, in a crystal, the atoms are close to each other (2 Å to 3 Å) and therefore the electrons intersect with each other and also with neighbouring atomic cores. The overlap (or interaction) will be more felt by the electrons in the outermost orbit while the inner orbit or core electron energies may remain unaffected. Therefore for understanding electron energies in Si or Ge crystal, we need to consider the changes in the energies of the electrons in the outermost orbit only. For Si the outermost orbit is the third orbit (n = 3), while for Ge it is the fourth orbit (n = 4). Each Si and Ge has four valence electrons, but Ge at a given temperature has more free electrons and a higher conductivity compared to Si. So, silicon is more widely used for semiconductor devices, since it can be used at much higher temperature than germanium.

(i) The energy of electrons of atoms of a substance will be same if

(a) atoms are isolated (b) atoms are closely spaced

(c) atoms are excited (d) atoms are charged

Sol. (a)

The electron energy will be same if all the atoms are isolated i.e., separated from each other by a large distance.

(ii) In a crystal, the distance between two atoms is

(a) 200 Å to 300 Å (b) 3 Å to 3 micron (c) 2 Å to 3 Å (d) 2mm to 3mm

Sol. (c)

In a crystal, the atoms are close to each tore (2 Å to 3 Å).

(iii) The overlap (or interaction) will be more felt by the electrons when they are

(a) in the outermost orbit (b) in the innermost orbit (c) free (d) in any orbit

Sol. (a)

The overlap (or interaction) will be more felt by the electrons in the outermost orbit while the inner orbit or core electron energies may remain unaffected.

(iv) For Silicon and Germanium he outermost orbits are respectively:

(a) n = 3 and n = 5 (b) n = 4 and n = 3 (c) n = 5 and n = 4 (d) n = 3 and n = 4

Sol. (d)

For Si the outermost orbit is the third orbit (n = 3), while for Ge it is the fourth orbit (n = 4).

(v) Why silicon is more widely used for semiconductor devices?

(a) It can be used at much higher temperatures than germanium.

(b) It is cheaper than germanium.

(c) It has higher conductivity than germanium.

(d) None of the above.

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Sol. (a)
Each Si and Ge has four valence electrons, but Ge at a given temperature has more free electrons and a higher conductivity compared to Si. So, silicon is more widely used for semiconductor devices, since it can be used at much higher temperature than germanium.

## E. ASSERTION REASON TYPE QUESTIONS

**(a) If both assertion and reason are true and reason is the correct explanation of assertion.**
**(b) If both assertion and reason are true but reason is not the correct explanation of assertion.**
**(c) If assertion is true but reason is false** **(d) If both assertion and reason are false**
**(e) If assertion is false but reason is true.**

1. Assertion: Ohm's law is obeyed in semiconductors at high electric field.
Reason: According to Ohm's law, voltage varies linearly with current.

Ans. (e) Assertion is false but reason is true.
In semiconductor, Ohm's law is obeyed only for low electric field (less than $10^6$ $Vm^{-1}$). Above the field the current becomes almost independent of applied field.

2. Assertion: Electron has higher mobility than hole in a semiconductor.
Reason: Mass of electron is less than the mass of hole.

Ans. (b) Both assertion and reason are true but reason is not the correct explanation of assertion.
Electrons move in conduction bands which are mostly empty so they encounter lesser resistance than holes moving in dense valence bonds.

3. Assertion: The crystalline solids have a sharp melting point.
Reason: All the bonds between the atoms of molecules of a crystalline solids are equally strong, that they get broken at the same time.

Ans. (a) Both assertion and reason are true and reason is the correct explanation of assertion.
At a particular temperature all the bonds of crystalline solids breaks and show sa\harp melting point.

4. Assertion: Silicon is preferred over germanium for making a semiconductor devices.
Reason: The energy band for germanium is more than the energy band of silicon.

Ans. (d) Both assertion and reason are false
The energy gap of germanium is less (0.72eV) than the energy gap (1.1eV). Therefore germanium is preferred over silicon for making semiconductor devices.

5. Assertion: The direction of diffusion current in a junction diode is from n region to p region.
Reason: The majority current carriers diffuse from a region of higher concentration to a region of lower concentration.

Ans. (e) Assertion is false but reason is true.

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The direction of diffusion current is that when positively charged particles move from p type to n type of diodes.

## F. CHALLENGING PROBLEMS

1. The number of silicon atoms per $m^3$ is 5 x $10^{28}$. This is doped simultaneously with 5 x $10^{22}$ atoms per $m^3$ of Arsenic and 5 x $10^{20}$ per $m^3$ atoms of Indium. Calculate the number of electrons and holes. Given that $n_i$ = 1.5 x $10^{16}$ $m^{-3}$. Is the material n-type or p- type?

Sol. Here $N_D = 5\times10^{22}$ $m^{-3}$; $N_A = 5\times10^{20} m^{-3}$, $n_i = 1.5\times10^{16} m^{-3}$.

For semiconductor to remain electrically neutral, $N_D - N_A = n_e - n_h$ …(1)

Also, $n_e n_h = n_i^2$

Therefore $(n_e + n_h)^2 = (n_e = n_h)^2 + 2n_e n_h = (N_D - N_A)^2 + 4n_i^2$ …(2)

$n_e + n_h = \sqrt{(N_D - N_A)^2 + 4n_i^2}$

Adding (1) and (2 ) we get

$n_e = \frac{1}{2}((N_D + N_A) + \sqrt{(N_D - N_A)^2 + 4n_i^2}$

$= \frac{1}{2}[(5 \times 10^{22} - 0.05 \times 10^{22}) + \sqrt{(4.95 + 10^{22})^2 + 4 \times (1.5 \times 10^{16})^2}]$

$= \frac{1}{2}[4.95 \times 10^{22} + \sqrt{(4.95 + 10^{22})^2} = 4.9\times10^{22}$ $m^{-3}$

$n_h = \frac{n_i^2}{n_e}$

$= \frac{(1.5\times10^{16})^2}{4.95\times10^{22}} = \frac{2.25\times10^{32}}{4.95\times10^{22}} = 4.5\times10^{9} m^{-3}$

As $n_e > n_h$ the material is of n type.

2. In an intrinsic semiconductor the energy gap $E_g$ is 1.2 eV. Its hole mobility is much smaller than electron mobility and independent of temperature. What is the ratio between conductivity at 600 K and that at 300 K ? Assume that the temperature dependence of intrinsic carrier concentration $n_i$ is given by

$$n_i = n_0 \exp\left(-\frac{E_g}{2k_B T}\right),$$

where $n_0$ is constant

Sol. As $\mu_e >> \mu_h$, and of intrinsic semiconductor $n_e = n_h = n_i$

Therefore conductivity is given by $\sigma = e(n_e\mu_e + n_h\mu_h) = en_i(\mu_e + \mu_h) = en_i\mu_e$ [since $\mu_e >> \mu_h$]

But $n_i = n_0 \exp\left[\frac{-E_g}{2k_B T}\right]$

Therefore $\sigma = e\mu_e n_0 \exp\left[\frac{-E_g}{2k_B T}\right]$

Here all the pre exponential terms are assumed independent of temperature. So we can put a constant$\sigma_0 = e\mu_e\mu_0$ and express the conductivity as $\sigma = \sigma_0 \exp\left[\frac{-E_g}{2k_BT}\right]$

Now $\frac{E_g}{2} = \frac{1.2}{2} = 0.6eV; k_B = 8.62\times10^{-5}\ eVK^{-1}$

Therefore $\sigma(600K) = \sigma_0 exp\left[\frac{-0.6}{8.62\times10^{-5}\times600}\right]$ and $\sigma(300K) = \sigma_0 exp\left[\frac{-0.6}{8.62\times10^{-5}\times300}\right]$

Hence $\frac{\sigma(600K)}{\sigma(300K)} = \frac{\exp\left[\frac{-0.6}{8.62\times10^{-5}\times600}\right]}{\exp\left[\frac{-0.6}{8.62\times10^{-5}\times300}\right]} = \exp\left[\frac{-0.6}{8.62\times10^{-5}}\left(\frac{1}{300}-\frac{1}{600}\right)\right]$

$= \exp\left[\frac{0.6\times10^5}{8.62\times600}\right] = \exp(11.6) = 1\times10^5$.

This shows that the conductivity of a semiconductor increases rapidly with the rise in temperature.

3. In a P-n junction diode, the current I can be expressed as

$$I = I_0 \exp((ev/2k_BT) - 1)$$

where $I_0$ is reverse saturation current. V is the voltage across the diode and is positive for forward bias and negative for reverse bias, and I is the current through the diode, $K_B$ is the Boltzmann constant ($8.6 \times 10^{-5}$ eV/K) and T is the absolute temperature. If for a given diode $I_0 = 5 \times 10^{-12}$ A and T = 300 K, then

(a) What will be the forward current at forward voltage of 0.6 V ?

(b) What will be the increase in current if voltage across diode is increased to 0.7 V ?

(c) What is the dynamic resistance?

(d) What will be the current if reverse bias voltage changes from 1 V to 2 V?

Sol. The current I through a junction is given as $I = I_0\left[\exp\left(\frac{eV}{2k_BT}\right) - 1\right]$

Where $I_0 = 5\times10^{-12}$A, T = 300K, $k_B = 8.6\times10^{-5}eVk^{-1} = 8.6\times10^{-5} \times1.6\times10^{-19}\ JK^{-1}$

(a) When V = 0.6V, $\frac{eV}{k_BT} = \frac{1.6\times10^{-19}\times0.6}{8.6\times1.6\times10^{-24}\times300} = \frac{600}{8.6\times3} = 23.26$

$\therefore I = I_0\left[\exp\left(\frac{eV}{2k_BT}\right) - 1\right] = 5\times10^{-12} \times [\exp(23.26) - 1]A = 5\times10^{-12}[1.2586 \times10^{10} - 1]A$

$= 5\times10^{-12}\times1.2586 \times10^{10}A = 0.06293A$

(b) When V = 0.7V, $\frac{eV}{k_BT} = \frac{1.6\times10^{-19}\times0.7}{8.6\times1.6\times10^{-24}} = 27.13$

$\therefore I = I_0\left[\exp\left(\frac{eV}{2k_BT}\right) - 1\right] = 5\times10^{-12} \times [\exp(27.13) - 1]A = 5\times10^{-12}[6.07 \times10^{11} - 1]A$

$= 5\times10^{-12}\times6.07 \times10^{11}A = 3.035A$

Increase in current, $\Delta I = 3.035 - 0.06293 = 2.972A$

(c) For $\Delta V = 0.7 - 0.6 = 0.1V$, $\Delta I = 2.9272A$

Dynamic resistance, $r_d = \frac{\Delta V}{\Delta I} = \frac{0.1}{2.972} = 0.0336\Omega$.

(d) For both the voltages, the current I will be almost equal to $I_0$ showing almost infinite dynamic resistance in the reverse bias.

$I = - I_0 = - 5\times10^{-12}A.$



**SPACE FOR ROUGH WORK**

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**SPACE FOR NOTES**

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